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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,739	03/16/2004	Richard W. Foote	P05819	1844

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EXAMINER	
TRAN, MAI HUONG C	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 09/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,739	FOOTE, RICHARD W.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Restriction is withdrawn and all claims, 1-20, are considered.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,648,281 to Williams et al.

Regarding to claim 1, Williams discloses a method for manufacturing a bipolar transistor of the type comprising a base 103, an emitter 168 and a collector 204 formed on a substrate 10, said method comprising the steps of etching a trench in said substrate between a first area for forming a base and an emitter (base/emitter area) and a second area for forming a sinker 19 and a collector 204; doping a portion of said substrate in said second area to form a sinker and collector layer comprising a sinker portion and a

collector portion (col. 16, lines 15-67, and col. 17, figs. 19-20); and establishing a value breakdown voltage for said bipolar transistor by causing a distance of said collector portion from said first area (base/emitter area) to have a selected value (col. 26, lines 10-67, cols. 27-28, and col. 29, lines 1-6).

Regarding to claim 2, the method wherein said step of doping a portion of said substrate to form a sinker and collector layer comprising a sinker portion and a collector portion comprises the steps of implanting dopant in a portion of said substrate at the bottom of said trench to create said collector portion of said sinker and collector layer; and implanting dopant in a portion of said substrate that is located adjacent to said collector portion but not in said trench to create said sinker portion of said sinker and collector layer (cols. 16-17).

Regarding to claim 3, the method further comprising the step of applying a heat treatment to diffuse dopant in said sinker portion into adjacent substrate areas and to diffuse dopant in said collector portion into adjacent substrate areas until said sinker portion and said collector portion are joined to form said sinker and collector layer (col. 24, lines 63-67, cols. 25-26).

Regarding to claim 4, the method further comprising the step of terminating said heat treatment when said dopant in said sinker portion diffuses laterally under said trench

to a desired distance from said first area (base/emitter area) (col. 24, lines 63-67, cols. 25-26).

Regarding to claim 5, the method further comprising the step of etching said trench to a depth that optimizes a value resistance of said bipolar transistor versus breakdown voltage of said bipolar transistor (col. 26, lines 10-67, cols. 27-28, and col. 29, lines 1-6).

Regarding to claim 6, the method wherein said step of establishing a value of breakdown voltage for said bipolar transistor by causing a distance of said collector portion from said first area (base/emitter area) to have a selected value comprises the steps of placing a collector and sinker mask over a portion of said trench that is adjacent to said first area; and selecting a lateral extent of a horizontal portion of said collector and sinker mask to control a distance of a subsequent lateral diffusion of said collector portion from said first area (base/emitter area) (col. 26, lines 10-67, cols. 27-28, and col. 29, lines 1-6).

Regarding to claim 7, the method wherein said lateral extent of said horizontal portion of said collector and sinker mask is selected so that a subsequent lateral diffusion of said collector portion does not extend into a portion of said substrate layer that is

located within a specified distance from a wall of said trench that is adjacent to said first area (base/emitter area) (col. 26, lines 10-67, cols. 27-28, and col. 29, lines 1-6).

Regarding to claim 8, the method wherein said specified distance is a distance that optimizes a value of resistance of said bipolar transistor versus breakdown voltage of said bipolar transistor (col. 26, lines 10-67, cols. 27-28, and col. 29, lines 1-6).

Regarding to claim 9, a bipolar transistor of the type comprising a base 103, an emitter 168 and a collector 204 formed on a substrate 10, said bipolar transistor comprising a trench etched in said substrate between a first area for forming a base and an emitter and a second area for forming a sinker and a collector; and a portion of said substrate in said second area doped to form a sinker and collector layer comprising a sinker portion 19 and a collector portion 204 (col. 16, lines 15-67, and col. 17, figs. 19-20); wherein a length of said collector portion is formed having a selected distance from said first area (base/emitter area) to establish a selected value of breakdown voltage for said bipolar transistor (col. 26, lines 10-67, cols. 27-28, and col. 29, lines 1-6).

Regarding to claim 10, the bipolar transistor wherein said sinker and collector layer comprises a portion of said substrate at the bottom of said trench that is doped to create said collector portion of said sinker and collector layer; and a portion of said

substrate that is located adjacent to said collector portion but not in said trench that doped to create said sinker portion of said sinker and collector layer (cols. 16-17).

Regarding to claim 11, the bipolar transistor further comprising said sinker portion having dopant diffused into adjacent substrate areas and said collector portion having dopant diffused into adjacent substrate areas wherein said diffused dopant joins said sinker portion and said collector portion to form said sinker and collector layer (col. 24, lines 63-67, cols. 25-26).

Regarding to claim 12, the bipolar transistor further comprising said collector portion having dopant that has diffused laterally under said trench to a desired distance from said first area (base/emitter area) (col. 24, lines 63-67, cols. 25-26).

Regarding to claim 13, the bipolar transistor wherein said trench is etched to a depth that optimizes a value of resistance of said bipolar transistor versus breakdown voltage of said bipolar transistor (col. 26, lines 10-67, cols. 27-28, and col. 29, lines 1-6).

Regarding to claim 14, the bipolar transistor wherein said distance of said collector portion that is formed having a selected distance from said first area (base/emitter area) establish a selected value of breakdown voltage for said bipolar transistor is determined by placing a collector and sinker mask over a portion of said

trench that is adjacent to said first area; and selecting a lateral spacing of a horizontal portion of said collector and sinker mask from said first area (base/emitter area) to control a length of a subsequent lateral diffusion of said collector portion (col. 26, lines 10-67, cols. 27-28, and col. 29, lines 1-6).

Regarding to claim 15, the bipolar transistor wherein said lateral spacing of said horizontal portion of said collector and sinker mask is selected so that a subsequent lateral diffusion of said collector portion does not extend into a portion of said substrate layer that is located within a specified distance from a wall of said trench that is adjacent to said first area (base/emitter area) (col. 26, lines 10-67, cols. 27-28, and col. 29, lines 1-6).

Regarding to claim 16, the bipolar transistor wherein said specified resistance of distance is a distance that optimizes a value of said bipolar transistor versus breakdown voltage of said bipolar transistor (col. 26, lines 10-67, cols. 27-28, and col. 29, lines 1-6).

Regarding to claim 17, a bipolar transistor of the type comprising a base, an emitter and a collector formed on a substrate, said bipolar transistor comprising a trench etched in said substrate between a first area for forming a base and an emitter (base/emitter area) and a second area for forming a sinker and a collector; and a sinker and collector layer comprising a sinker portion and a collector portion formed by doping

a portion of said substrate; wherein a value of breakdown voltage for said bipolar transistor is determined by a distance of said collector portion from said first area (base/emitter area) (col. 16, lines 15-67, and col. 17, figs. 19-20, col. 26, lines 10-67, cols. 27-28, and col. 29, lines 1-6).

Regarding to claim 18, the bipolar transistor wherein lateral diffusion of dopant in said collector portion determines said distance of said collector portion from said first area (base/collector area) (col. 24, lines 63-67, cols. 25-26).

Regarding to claim 19, the bipolar transistor wherein said dopant in said collector portion at the bottom of said trench is laterally diffused under said trench by heat treatment (col. 24, lines 63-67, cols. 25-26).

Regarding to claim 20. The bipolar transistor as set forth in Claim 18 wherein a distance of said collector portion before dopant in said collector portion laterally diffuses is determined by a length of a horizontal portion of a collector and sinker mask (col. 26, lines 10-67, cols. 27-28, and col. 29, lines 1-6).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran